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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/001,477	ROE ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-14 and 17-20 were rejected in the Office Action of 24 August 2006.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 22 November 2006 has been entered.

Applicants' submission filed on 22 November 2006 has amended claim 17 and presented new claims 21-23. Claims 1-14 and 17-23 are pending in this application.

Claims 1-14 and 17-23 are rejected.

Priority

1. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is denied, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. § 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the Application. In particular, no part of the provisional application appears to disclose the method steps shown in the Application at Fig. 7.

Claim Objections

2. The previous objection to claim 17 has been withdrawn in response to Applicants' amendments.

Double Patenting

3. Claims 1, 7, and 14 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 13 of copending Application No. 09/975,338. Although the conflicting claims are not identical, they are not patentably distinct from each other because where the limitations of claim 13 of the copending application only differ semantically from the independent claims 1, 7, and 14 of the instant application. Where claims from copending applications cover the same subject matter but are claimed slightly differently, it would have been obvious to a person of ordinary skill in the art to claim the invention in slightly different terms as exhibited the conflicting claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Applicants' response on 12 December 2005 states that Applicants will correspond to the provisional double patenting rejection upon an indication of allowance of subject matter of either the present application or the co-pending application (09/975,338).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 21-23 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 21-23 recite the phrase "said virtual microcontroller functions *substantially identical* to said microcontroller" which is vague and indefinite. The phrase "substantially identical" is used here as a relative term that is not clearly defined. It is unclear how close to "identical" the virtual microcontroller's functionality must be to the microcontroller in order to fall under the scope of this claim language.

Claims 21-23 recite the phrase "debugging related functions on said microcontroller is *minimized*" which is vague and indefinite. It is unclear how to analyze the prior art and conclude that debugging related functions have been "minimized," and if so, whether they fall under the scope of the claim language.

Response to Arguments

In response to the previous rejections of claims 1-14 and 17-20 under 35 U.S.C. § 103 as being unpatentable over Marik in view of Grunert, Applicants argue primarily that:

> Therefore, Marik discloses a table containing only information regarding interrupts associated with the target system. According, the table in Marik fails to include break bits associated with instruction addresses where no break is to occur. Therefore, Marik fails to teach or suggest a break bit associated with each of a plurality of instruction addresses, as claimed.

The Examiner respectfully traverses this argument as follows.

The claim language does not require "break bits associated with instruction addresses where no break is to occur," as implied by Applicants' arguments. The claim language does

require "a break bit associated with each of a plurality of instruction addresses," which is shown in Marik. Specifically, a plurality of instruction addresses are present in the table. A "Boolean flag for breaking," i.e. a break bit, is associated with each of the plurality of instruction addresses present in the table (support as cited in the rejection). The break bit in Marik is set to indicate that a break is to occur at a specified instruction address.

Additionally, Marik expressly teaches that the "Boolean flag for breaking" may be set to "0"=disabled (column 6, line 67). Therefore, although there is no requirement for such a feature in the claim language, Marik expressly teaches "break bits associated with instruction addresses where no break is to occur."

Applicants further argue that:

> Marik discloses that a microcontroller receives a debugger signal as an interrupt input but it fails to explicitly teach or suggest a breakpoint controller sending a break message, as claimed.

The Examiner respectfully traverses this argument as follows.

In Applicants' terminology, the break message originates from a "breakpoint controller". In Marik, the break message originates from the INT0 interrupt handler. Applicants have not distinguished the structure or function of the claimed "breakpoint controller" from the INT0 interrupt handler in Marik. Therefore there appears to be no difference between the prior art reference and the claimed invention except in terminology.

Applicants submit that:

> The Office Action recites Marik (column 14, lines 19-35) to show the breakpoint controller that sends a break message to the microcontroller whenever an instruction address is encountered that is associated with a set break bit, as claimed. The Applicants, however, do not understand the disclosed portion of Marik to correspond to what has been quoted by the Examiner. Accordingly, clarification in the next Office Action is requested if the rejection is maintained.

The citation in the previous Office Action included a typographical error. The portion of the Marik reference which the Examiner has quoted in the rejection comes from (column 16, lines 19-35). The Examiner apologizes for any confusion caused by this error.

Applicants further argue that:

> Marik discloses that "what is needed is a debugging method and system that performs the emulator debugging functions on an off-the-shelf microcontroller in place in the system under test without the need for in-circuit emulator technology (cit. omitted) ... In contrast, Grunert is a circuit arrangement for in-circuit emulation of a microcontroller (cit. omitted) to reduce the outlay for providing a microcontroller suitable for in-circuit emulation (cit. omitted) ... Accordingly, the addition of Grunert to Marik renders Marik inoperable and the addition of Marik to Grunert renders Grunert inoperable. Accordingly, the cited references are incapable of the asserted combination.

The Examiner respectfully traverses this argument as follows.

In the previous Office Action, the rejection under 35 U.S.C. § 103 referred to a physical combination of Marik's system and Grunert's microcontroller. In response, Applicants' arguments rely upon Marik's motivation for invention (*a debugging method and system ... without the need for in-circuit emulator technology*) as conclusive evidence that combination with Grunert's in-circuit emulator would be inoperable. The Examiner submits that the facts simply do not support this conclusion. This argument is unpersuasive.

In this Office Action, the rejection under 35 U.S.C. § 103 set forth below identifies that the claimed invention is obvious over a combination of the teachings found in the prior art references, and does not cite a bodily incorporation of physical components found in the prior art. The Examiner submits that there is no evidence in either of these references to support a conclusion that the combination of their teachings would result in an inoperable device.

Applicants further argue that:

> Marik teaches away the recited limitations of independent claim 1 because Claim 1 is directed to an in-circuit emulation system, as claimed whereas Marik is directed to a debugging method and system without in-circuit emulation technology.

The Examiner respectfully traverses this argument as follows.

Marik teaches a system that achieves the functionality of an in-circuit emulation system without additional "in-circuit emulator technology, additional microcontroller on-board circuitry, or a supporting microcontroller designed into the system under test" (column 2, lines 14-19). That is, the **object of Marik's invention is to enhance in-circuit emulation** by using fewer components. Marik plainly does not "teach away" from in-circuit emulation.

Applicants' arguments for independent claim 7 and 14 and the dependent claims refer back to these arguments presented in reference to claim 1. These arguments have been addressed above.

Applicants' arguments have been fully considered but have been found unpersuasive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

5. Claims 1-14 and 17-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,903,718 to Marik in view of US Patent No. 6,366,878 to Grunert.

Regarding claim 1, Marik teaches:

An in-circuit emulation system [*"The Debug Tool of a preferred embodiment of the present invention is a 8031 debug tool with emulator types of functions which needs only a minicomputer, such as a PC, running a user-interactive PC Host Debugger Application program and a serial cable attaching the standard communication port of a PC to the 8031 based target system."* (column 3, line 66 – column 4, line 4)] breakpoint control [*"Debug Parameter Table"* (column 6, lines 48 *et seq.*)] comprising:

A microcontroller [*"According to the present invention, a remote program monitor method and system using a system-under-test microcontroller for self-debug comprises a system-under-test (SUT_ that includes a read-only memory (ROM) and a microcontroller for executing a program under test."* (column 2, lines 22-27)];

A breakpoint lookup table with a break bit associated with each of a plurality of instruction addresses, the break bit being set to indicate that a break is to occur at a specified instruction address [*"The Debug Parameter Table contains a record for each specified debugpoint in the target system. Each record consists of: 1) A program memory address which is compared to the target system program counter at the time the debugpoint occurs. If a match occurs, the debugpoint takes action based upon the contents of the remainder of this record."* (column 6, lines 48-61)];

A breakpoint controller that sends a break message to the microcontroller whenever an instruction address is encountered that is associated with a set break bit [*"When the SUT receives one or more debugger signals as an interrupt input, the signal causes the microcontroller to execute a debugger program contained in the ROM."* (column 2, lines 22-38); *"When a debugpoint is reached, the INT0 interrupt handler checks the Debug Parameter Table to verify that the breakpoint is enabled. A break is enabled if the Break Boolean flag is set true and the program counter value in the Debug Parameter Table matches the program counter at the top of the stack upon entry into the INT0 interrupt handler."* (column 16, lines 19-35)].

Marik does not disclose a virtual microcontroller operating in lock-step synchronization with the microcontroller by virtue of their identical operation.

Grunert teaches a virtual microcontroller operating in lock-step synchronization with a microcontroller by virtue of their identical operation [*"The arrangement, according to the invention, for in-circuit emulation comprises two identical microcontrollers, which are operated*

as master and slave, as well as the external program memory. The slave receives the same program instructions parallel to the master." (column 1, lines 47-65); *"In accordance with another feature of the invention, a clock synchronizes the two microcontrollers (2, 3)."* (column 2, lines 58-59)].

Grunert and Marik are analogous art because both are directed to microcontroller development and testing.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of the virtual microcontroller operating in lock-step synchronization with the teachings of Marik's debugging system to arrive at the claimed invention. The combination would involve the desirable features of Marik's debugging system with the desirable features of Grunert's virtual microcontroller system.

The motivation for doing so would be to achieve better visibility into the internal operations of the microcontroller, as expressly taught by Grunert [*"In accordance with an advantageous feature of the present invention, the operating program for in-circuit emulation is not stored in the internal ROM memory, but in an external, and therefore easily accessible memory."* (Grunert, column 1, lines 36-47); *"Internal states of the master 2 are transmitted to the slave 3 via the ports P3, P4', and then to the service computer via the ports P5', P6',.... The contents of the memory 4 can be changed by the service computer, in order to optimize the microcontroller in the application system during the development phase. The internal state of the master 2 can be traced by setting breakpoints. The service computer executes the application program in this case in parallel with the execution in the master 2."* (Grunert, column 5, lines 10-25)].

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the Marik and Grunert references to obtain the invention specified in claim 1.

Regarding claim 2, Grunert teaches that messages are sent to the microcontroller over an interface linking the (master) microcontroller to the (slave) virtual microcontroller [*"A signal connection between the microcontrollers 2, 3 is produced by port P3 in the master and port P4' in the slave. The respective settings of the connecting devices 9, 9' ensure that the ports P0', P2', P3' of the slave 3 are switched through to the master 2 so that all the input and output data of the function unit 7 are available in the master 2 as in normal operation."* (column 4, lines 63-67); *"The corresponding ports P5', P6' are therefore free in the slave 3, with the result that they can be used for inputting and outputting further internal signals and states, for example internal buses, control signals, register contents, etc. or for controlling the program execution."* (column 5, lines 10-25)].

Regarding claim 3, Marik teaches a counter that increments through the breakpoint lookup table as a sequence of instructions is executed [*"The Debugger Routine compares the program counter at the top of the stack upon entry into the INT0 Reentrant Routine with the program counter field of each record in the DPT until a match is found. If a match is found, the "active" DPT record is replaced by the new matched record. The debug Boolean flags in the DPT record dictate what action is to be taken."* (column 14, lines 59-65)]

Regarding claim 4, Marik teaches a host computer that programs the breakpoint lookup table to set a breakpoint bit at an instruction address where a break is to occur [*"To selectively disable or enable debugpoints, the PC host 10 can update the Debug Parameter Table of Boolean flags."* (column 15, line 50 – column 16, line 3); *"Initially, the target system 8031 source code is assembled on the PC."* (column 8, lines 4-22); *"Included in the assembly of the target system source code is the Debug Parameter Table and "enable INT0 interrupt" instructions placed at strategic locations where debugpoints are desired."* (column 8, lines 34-52)].

Regarding claim 5, Grunert teaches that the microcontroller and the virtual microcontroller operate in a two phase cycle comprising a control phase and a data transfer phase [control phase: *"The corresponding ports P5', P6', are therefore free in the salve 3, with the result that they can be used for inputting and outputting further internal signals and states, for example internal buses, control signals, register contents, etc. or for controlling the program execution."* (column 5, lines 10-25); data transfer phase: *"Internal states of the master 2 are transmitted to the slave 3 via the ports P3, P4', and then to the service computer via the ports P5', P6', ... The contents of the memory 4 can be changed by the service computer, in order to optimize the microcontroller in the application system during the development phase."* (column 5, lines 10-25)].

Regarding claim 6, Grunert teaches that the break message is sent during the control phase [*"The corresponding ports P5', P6', are therefore free in the salve 3, with the result that*

they can be used for inputting and outputting further internal signals and states, for example internal buses, control signals, register contents, etc. or for controlling the program execution." (column 5, lines 10-25); *"The internal state of the master 2 can be traced by setting breakpoints."* (column 5, lines 10-25)].

Regarding claim 21, Grunert teaches that the microcontrollers are identical [*"two identical microcontrollers"* (column 1, lines 48-51)].

Claims 7-10, 12-13, and 22 recite combinations of limitations found in claims 1-6 and 21. As claims 1-6 and 21 are obvious over Marik in view of Grunert, claims 7-10, 12-13, and 22 are similarly obvious over Marik in view of Grunert.

Regarding claim 11, Marik teaches halting execution of instructions in the microcontroller prior to the instruction associated with the set break bit [*"When a debugpoint is reached, the INT0 interrupt handler checks the Debug Parameter Table to verify that the breakpoint is enabled... The INT0 routine will then invoke the Communication API to transfer the contents of the trace table to the PC host 10 for display, then query the Communication API for a message from the PC host 10 to continue processing the target system code 40."* (column 16, lines 19-35)].

Claims 14, 17-20, and 23 recite combinations of limitations found in claims 7-13 and 22. As claims 7-13 and 22 are obvious over Marik in view of Grunert, claims 14, 17-20, and 23 are similarly obvious over Marik in view of Grunert.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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1/17/07